10. (Currently Amended) A method of manufacturing a flat panel display device, comprising:

forming a semiconductor layer on an insulating layer;

ion-implanting an impurity having a first conductivity into the semiconductor layer;

forming a source electrode and a drain electrodes, the source electrode contacting a first end portion of the semiconductor layer and the drain electrodes ~~directly~~ contacting ~~a first end portion and~~ a second end portion of the semiconductor layer;

ion implanting an impurity having a second conductivity into the semiconductor layer to form a high-density source region, ~~and~~ a high-density drain regions and a channel area, the high-density source region contacting the source electrode and the high-density drain regions ~~directly~~ contacting the ~~source and~~ drain electrodes;

forming a first insulting layer over ~~an entire~~ surface of the insulating substrate;

forming a pixel electrode having an opening formed thereon; and

forming a gate electrode on a portion of the first insulating layer formed over the semiconductor layer.

11. (Currently Amended) The method of claim 10, wherein the source electrode and the drain electrodes include a pixel electrode material layer, a metal material layer and a capping insulating material layer, each stacked sequentially.

12. (Original) The method of claim 10, wherein the pixel electrode exposed through the opening portion is formed by sequentially etching the first insulating layer, a capping insulating layer and a metal material layer, each stacked sequentially.

13. (Currently Amended) The method of claim 12, further comprising, a storage capacitor including first capacitor electrode and a second capacitor electrodes with a dielectric layer interposed therebetween, the first capacitor electrode extending from either of the source electrode and the drain electrodes and including the pixel electrode material layer and the metal material layer, each stacked sequentially, the second capacitor electrode including a gate electrode material layer, the dielectric layer electrode formed on the first capacitor electrode and including the capping insulating layer and the first insulating layer, each stacked sequentially.

14. (Original) The method of claim 13, further comprising, forming a contact hole contemporaneously with forming the pixel electrode having the opening portion, the contact hole contacting the first capacitor electrode and the gate electrode.

15. (New) The method of claim 10, wherein the first source electrode directly contacts the first end portion of the semiconductor layer and the second source electrode directly contacts the second end portion of the semiconductor layer.

16. (New) The method of claim 10, wherein the first insulting layer is formed over an entire surface of the insulating substrate.

17. (New) The method of claim 10, wherein the high-density source region directly contacts the source electrode and the high-density drain region directly contacts the drain electrode.